UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,017	04/08/2004	Jian H. Jiang	073338.0176 (04-50096 FLA	9311

5073 7590 04/14/2005

BAKER BOTTS L.L.P.
2001 ROSS AVENUE
SUITE 600
DALLAS, TX 75201-2980

EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/821,017	JIANG, JIAN H.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-20* is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 14-17* is/are rejected.

7)☒ Claim(s) *6 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 2, 9 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the limitation "the difference between the maximum values of the high and low voltage domains by at least a factor of two" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out/explain how this limitation reads on the circuit arrangement.

Claims 9 and 16 are similarly rejected as claim 2.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 8-10, 12 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Clark et al (U.S Patent No. 6,774,696).

Clark et al disclose in Figs. 1-5 a level shifter and voltage translator including:

Regarding claim 1:

receiving an input signal (signal applied to block 520) in a low voltage domain (510); and

using the input signal (the signal applied to block 520,i.e, DROWSY, SIGNAL FROM POWER DOWN DOMAIN), controlling a first transistor (150) having a first carrier type (P-channel MOS), a second transistor (140) having a second carrier type (N-channel MOS) different from the first carrier type (P-channel MOS), and a third transistor (130) having the second carrier type (N-channel MOS) to produce an output voltage at an output terminal (145), wherein:

the first transistor (150) is coupled to the output terminal (145) and further coupled to a first voltage corresponding to a first value in a high voltage domain (180);

the second and third transistors (140 and 130) are coupled in series between the output terminal (145) and a second voltage corresponding to a second value in the high voltage domain (Ground); and

the output voltage (voltage at 145) is selected to correspond to either the first voltage or the second voltage based upon the input signal (DROWSY, SIGNAL FROM POWER DOWN DOMAIN).

Regarding claim 2: amplifying (420) the output voltage (v145) by an amount of voltage less than the difference between the maximum values of the high and low voltage domains (difference between VHIGH – VLOW) at least a factor of two (due to indefiniteness, the limitation "at least a factor of two" can not given sufficient weight to read over the reference).

Regarding claim 3: elements PMOS connected to POWER DOWN(PD), NMOS connected to POWER DOWN BAR, and LOW VOLTAGE DOMAIN (MTCMOS) read on a logical gate operate to apply a logical operation to the input signal (signal applied to block 520).

Regarding claim 5: the steps of controlling comprises applying the input signal to at least one control transistor (110) operable to control at least one of the second and third transistors (130).

Claim 8 is similarly rejected as claim 1:

a receiver operable to receive an input signal in a low voltage domain (510); and

a first transistor (150) having a first carrier type (P channel MOS), wherein the first transistor (150) is coupled to the output terminal (145) and further coupled to a first voltage corresponding to a first value in high voltage domain (180);

a second transistor (140) having a second carrier type (N channel MOS) different from the first carrier type (P channel MOS);

a third transistor (130) having the second carrier type (N channel MOS), wherein the second and third transistors (140, 130) are coupled in series between the output terminal (145) and a second voltage (Ground) corresponding to a second value in the high voltage domain; and

a control structure (110, 120) operable to control the first, second and third transistors (150, 140, 130) to produce an output terminal (145) corresponding to either the first voltage or the second voltage in response to the input signal (DROWSY, SIGNAL FROM POWER DOWM DOMAIN).

Claim 9 is similarly rejected as claim 2.

Claim 10 is similarly rejected as claim 3.

Claim 12 is similarly rejected as claim 5.

Claim 15 is similarly rejected as claims 1 and 8.

Claim 16 is similarly rejected as claim 9.

Claim 17 is similarly rejected as claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 7, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al as applied to claim 1 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Clark et al. However, this reference does not specifically show the "the high value of the low voltage domain is 1.25V and the high value of the high voltage domain is 2.5V" recited in claims 4 and 11 and "the input signal has a frequency greater than 1 gigahertz" recited in claims 7 and 14.

Although Clark et al do not expressly state the voltage value for the low and high voltage domains, this difference is not of patentable merit because it is notoriously well known in the art that different values for the voltage potential can be selected in order to

produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the high value for the low voltage domain is 1.25V and the high value of the high voltage domain is 2.5V in realizing the circuit of the Clark et al reference for the purpose of producing different output values when different values of the voltage potential is selected.

The same motivation applied to claims 4 and 11 is applied to claims 7 and 14: It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the input signal has a frequency greater than 1 gigahertz in realizing the circuit of the Clark et al reference for the purpose of providing high accuracy and improving the output performance of the circuit.

Allowable Subject Matter

Claims 6, 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 18-20 are allowable over the prior art of record. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: the combination of "an inverted NAND gate", "an inverter" and "first – fifth transistors" as recited in claim 18.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

April 11, 2005